Kontron User's Guide

X-board® <PXA>

Document Revision 1.17

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1 User Information

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Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 INTRODUCTION

2.1 X-board® Benefits

The X-board® modules of Kontron Embedded Modules GmbH are very compact (49mm x 68mm x 6mm) and highly integrated computers. All X-board® modules have a standardized form factor and a standardized connector (DDR-SODIMM Memory Connector) that carries a specified set of signals. This standardization allows designers to create a single system “baseboard” which can accept a variety of present and future X-board® modules.

X-board® modules include common personal computer (PC) peripheral functions such as serial ports, Ethernet, IDE, USB, etc.

The baseboard designer can optimize exactly how each of these functions is physically implemented. Connectors can be placed precisely where they are needed for the application, on a baseboard designed to optimally fit the system configuration and layout.

Legacy devices are omitted to reach a maximum in compactness and size.

Peripheral PCI or LPC devices can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard, using the computer as one “plug in” component, simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design may be used with a range of X-board® modules. This flexibility can be used to differentiate products at various price/performance points, or to design “future proof” systems that have a built-in upgrade path. The modularity of an X-board® solution also insures against obsolescence as computer technology continues to evolve. A properly designed X-board® baseboard can be used with several successive generations of X-board® modules.

An X-board® baseboard design thus has many of the advantages of a custom computer board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

2.2 X-board® Documentation

This manual is intended as one of three principal references for an X-board® design.

- The X-board® specification defines the X-board® module form factor, pinout and signals. It is suggested that this be read first.
- The design guide is intended as a general guide for baseboard design, with a focus on maximum flexibility in order to accommodate a wide range of X-board® modules.
- Finally, the technical manuals for specific X-board® modules document the specifications and features of each individual X-board® module.

3 Specifications

3.1 Functional Specifications

- Processor: Intel® XScale™ PXA255
- Bus: 100MHz bus clock
- Cache: 32KB integrated instruction and data cache
- Companion and Bridge Chipset: ITE IT8152G
- Onboard SDRAM with 16/32/64MB and Flash Memory with 8/16/32MB
- Two Serial Ports (COM1 and COM2)
  - Transistor-to-transistor (TTL) signals
- Intelligent Drive Electronics (IDE):
  - Programmed Input/Output (PIO) mode supported
- Universal Serial Bus (USB)
  - Three USB 1.1 ports (two host and one device)
- Peripheral Component Interconnect Bus (PCI, Version 2.1 compliant)
- Low Pin Count Bus (LPC, Version 1.0 compliant)
- Onboard Ethernet: Realtek RTL8100BL PCI single chip
  - 10BASE-T/100BASE-T LAN
  - Fast Ethernet NIC controller
- Onboard TFT and STN display driver integrated in Intel® XScale™ PXA255
  - Resolution up to 800x600 pixels (recommended maximum of 640x480)
  - 64k color / 256 Gray scale levels
- Audio: Integrated AC'97 Interface on Intel® XScale™ PXA255
  - AC'97 Rev 2.0 Interface to connect an AC'97 codec
- MMC Interface
- Several GPIO's
- Watchdog timer (WDT)

Note: This feature is not available on<PXA> modules up to PRev: ?X2.

- JTAG interface for easy debugging

3.2 Mechanical Specifications

3.2.1 Dimensions

- 49.0 mm x 68.0 mm

Height approx. 6 mm

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 3.3V DC +/- 5%

3.3.2 Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

3.3.3 Supply Current

- 420 mA

It was measured with a board with 64 MB RAM connected in a backplane without additional power consuming components.

3.4 Environmental Specifications

3.4.1 Temperature

- Operating: 0 to +70°C
- Non operating: -10 to +85°C

Note: *The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

4 CPU, COMPANION and Bridge CHIPset

4.1 Processor Intel® XScale™ PXA255

Intel® XScale™ PXA255 application processor is a 32-bit RISC based processor incorporating Intel's XScale™ Micro architecture based on the ARM* V5TE architecture.

- ARM* Architecture Version 5TE ISA compliant
  - ARM* Thumb Instruction Support
  - ARM* DSP Enhanced Instructions
- 32KB Instruction Cache / 32kB Data Cache / 2 KB "mini" Data Cache, Extensive Data Buffering
- Instruction and Data Memory Management Units
- Branch Target Buffer
- Intel® Media Processing Technology
  - Enhanced 16-bit Multiply
  - 40-bit Accumulator
- AC97 Controller
- USB Client Controller
- SDRAM interface tightly coupled to CPU core and graphics subsystem for maximum efficiency
- High Speed UART
- Fast infrared COM port
- Low power modes
- Companion Chip Interface
- MMC Controller
- Synchronous Serial Port (SSP)
- I2C Interface
- LCD Controller for STN and TFT displays
- General Purpose I/O ports
- DMA Controller

4.2 Companion and Bridge Chipset ITE IT8152G

The IT8152F is a companion chip, which interfaces directly to RISC processors, and provides a bridge to link host bus and PCI bus. It also provides Low Pin Count (LPC) host controller, interrupt controller and a DMA controller.

- PCI Bus Controller

- 32-bit data bus interface
- Supports PCI rev. 2.1 specification
- 33 MHz bus operation

➤ Low Pin Count (LPC) Host Controller

- Compliant with Intel LPC Interface Specification Rev. 1.0
- Supports I/O Read, I/O Write cycles
- Supports SYNC Time-out abort report
- Supports Error report
- No support of DMA and no memory I/O

➤ USB Host Controller

- Supports two USB ports
- Fully compatible with USB specification version 1.1
- Register compatible with OHCI specification version 1.0

5 System and flash memory

5.1 SDRAM

The X-board®<PXA> uses onboard Synchronous Dynamic Random Access Memory (SDRAM) sizes of 16, 32 or 64MB.

5.2 Flash

The X-board®<PXA> is optionally equipped with 8, 16 or 32MB Flash memory.

6 Interfaces

6.1 PCI Bus

The implementation of this subsystem complies with the *X-board®* Specification. Implementation information is provided in the *X-board® Design Guide*. Refer to the documentation for additional information.

6.2 LPC Bus

The implementation of this subsystem complies with the *X-board®* Specification. Implementation information is provided in the *X-board® Design Guide*. Refer to the documentation for additional information.

Note: ** If the LPC interface is not used on the customer's Backplane, the Signals LAD[0..3] and LDRQ# have to be connected together and pulled-up to 3.3V with an 15kΩ resistor.*

6.3 IDE Port (PIO Mode)

The implementation of this subsystem complies only in PIO Mode with the *X-board® Specification*. Implementation information is provided in the *X-board® Design Guide*. Refer to those documents for additional information.

6.4 Serial ATA Signals

Serial ATA is not supported on the X-board<PXA>

6.5 Serial Ports (COM1 and COM2)

The implementation of the serial-communication interface is restricted. COM1 supports all UART signals RXD, TXD, DTR#, CTS#, RTS#, DCD#, RI, DSR#, COM2 includes RXD, TXD, RTS# and CTS#. Implementation information is provided in the *X-board® Design Guide*. Refer to the documentation for additional information.

Configuration

The serial-communication interfaces are Intel® XScale™ PXA255 internal devices. The COM1 port is hardwired to the PXA255 FFUART, the COM2 port to the PXA255 BTUART.

6.6 USB

Two OHCI-type USB host controllers and one device controller are supported on the X-board®<PXA> module. The USB controllers comply with Version 1.1 of the USB standard. The implementation of this subsystem complies with the *X-board® Specification*. Implementation information is provided in the *X-board® Design Guide*. Refer to those documents for additional information.

Configuration

The USB controllers are PCI bus devices. The used operating system allocates required system resources during configuration of the PCI bus.

6.7 Ethernet

The Realtek RTL8100BL PCI is a cost-effective 10BASE-T/100BASE-TX LAN solution. It is designed for low-power use and high-performance processes. It is a 3.3V device with 5V tolerance and supports 3.3V and 5V signaling.

Configuration

The Ethernet interface is a PCI device. The operating system will automatically configure this controller.

Note: *The Ethernet interface works according to the common criteria of the embedded technology market segment.*

6.8 AC'97 Codec Interface

The sound function on the *X-board®<PXA>* board comes from the AC'97 interface of the Intel® XScale™ PXA255. An external Codec must be connected on the baseboard to use the audio functions. Please look at the implementation information provided in the *X-board® Design Guide*.

Configuration

The audio controller is an internal interface of Intel® XScale™ PXA255. The operating system will allocate required system resources during startup.

6.9 VGA Output

The PXA255 includes the display subsystem:

The LCD Controller supports both passive (DSTN) and active (TFT) flat-panel displays with a maximum supported resolution of 800x600x16-bit/pixel (recommended maximum of 640x480). An internal 256-entry palette expands 1, 2, 4, or 8-bit encoded pixels. Non-encoded 16-bit pixels bypass the palette.

Two dedicated DMA channels allow the LCD Controller to support single- and dual-panel displays. Passive monochrome mode supports up to 256 gray-scale levels and passive color mode supports up to 64K colors. Active color mode supports up to 64K colors.

6.10 Digital Flat Panel Interface

The *X-board®<PXA>* supports the Intelligent LCD Interface **(referred to as either JIDI or JILI-d)**. It provides the possibility to store controller specific panel configuration data in an external EEPROM.

Please contact Kontron Embedded Modules Technical Support for more information.

6.11 Television Output

The *X-board®<PXA>* does not support television output.

6.12 SMB/I2C BUS

The X-board®<PXA> provides only the I²C bus on that interface. The Intel® XScale™ PXA255 internal I²C controller is used.

6.13 Power Control

6.13.1 Power Good / Reset Input

The *X-board®<PXA>* provides an external input for a power good signal or a manual reset pushbutton. The implementation of this subsystem complies with the *X-board® Specification*. Implementation information is provided in the *X-board® Design Guide*. Refer to those documents for additional information.

6.14 Power Management

6.14.1 ATX PS Control

The X-board®<PXA> can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the *X-board® Specification*. Implementation information is provided in the *X-board® Design Guide*. Refer to those documents for additional information.

6.15 Watchdog Timer

This feature is implemented in the Intel® XScale™ PXA255. The Watchdog can be configured in the customer application to start after a set amount of time following power-on boot. The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

The watchdog can be programmed using the Standard JIDA32 Library API in a board and OS independent manner. Please refer to the JIDA32 Library API documentation. For hardware low level programming please refer to the Intel® XScale™ PXA255 manual.

Note: *The Watchdog Timer is not available on<PXA> modules with PRev: ?X2 or earlier.*

7 Limitations

7.1 PCI

GNT2#/REQ2# are used by Ethernet, therefore not available for external PCI devices.

7.2 Watchdog

The Watchdog only allows RESET, no NMI operation.

Note: *The Watchdog is not available on<PXA> modules with PRev: ?X2 or earlier.*

7.3 Keyboard / Mouse usage

You can either use a USB mouse and keyboard, or a PS/2 mouse and keyboard. Once a USB mouse or USB keyboard is plugged in, PS/2 devices are disabled.

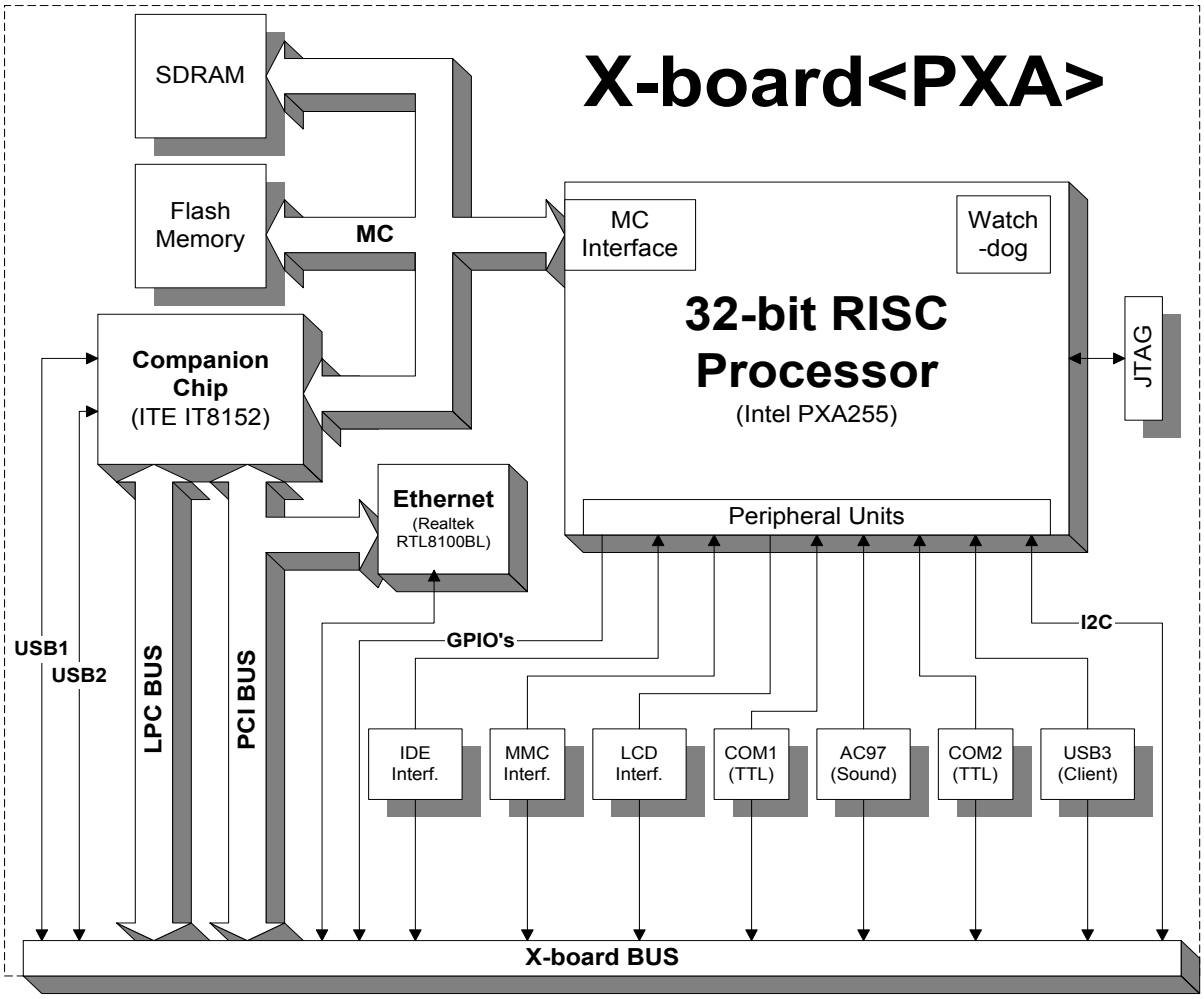
7.4 I²C Bus

The I²C bus is also used for JILI/JILI-d devices, therefore there may be additional devices (JILI Data EEPROM, Backlight DAC) reducing the number of available addresses. Please refer to the JILI manual to find out which addresses may not be available.

7.5 LPC

No support of DMA and no memory I/O.

8 Appendix a: block diagram



9 Appendix B: System Resources

9.1 Memory Area

Address Range [hex]	Resource Size	Function	Note
0000 0000 – 03FF FFFF	CS0 – 64 MB	Flash Bank 0	8 / 16 / 32 MB Flash
0400 0000 – 07FF FFFF	CS1 – 64 MB	N.U.	
0800 0000 – 0BFF FFFF	CS2 – 64 MB	N.U.	
0C00 0000 – 0FFF FFFF	CS3 – 64 MB	CPLD	
1000 0000 – 13FF FFFF	CS4 – 64 MB	ITE8152 companion	PCI memory, regs, IOs
1400 0000 – 17FF FFFF	CS5 – 64 MB	ITE8152 companion	PCI memory space
1800 0000 – 1BFF FFFF	64 MB	RESERVED	
1C00 0000 – 1FFF FFFF	64 MB	RESERVED	
2000 0000 – 2FFF FFFF	256 MB	N.U.	
3000 0000 – 3FFF FFFF	256 MB	N.U.	
4000 0000 – 43FF FFFF	64 MB	Memory-Mapped (MM) Registers (peripherals)	
4400 0000 – 47FF FFFF	64 MB	MM Registers (LCD)	
4800 0000 – 4BFF FFFF	64 MB	MM Registers (Memory Ctrl)	
4C00 0000 – 4FFF FFFF	64 MB	RESERVED	
5000 0000 – 5FFF FFFF	256 MB	RESERVED	
6000 0000 – 6FFF FFFF	256 MB	RESERVED	
7000 0000 – 7FFF FFFF	256 MB	RESERVED	
8000 0000 – 8FFF FFFF	256 MB	RESERVED	
9000 0000 – 9FFF FFFF	256 MB	RESERVED	
A000 0000 – A3FF FFFF	64 MB	SDRAM – partition 0	nSDCS_0
A400 0000 – A7FF FFFF	64 MB	N.U.	
A800 0000 – ABFF FFFF	64 MB	N.U.	
AC00 0000 – AFFF FFFF	64 MB	N.U.	
B000 0000 – BFFF FFFF	256 MB	RESERVED	
C000 0000 – CFFF FFFF	256 MB	RESERVED	
D000 0000 – DFFF FFFF	256 MB	RESERVED	
E000 0000 – EFFF FFFF	256 MB	RESERVED	

9.2 Peripheral Component Interconnect (PCI) Devices

PCI Device	PCI Interrupt	Comment
Ethernet	INTC	Use REQ2/GNT2 pair

You can use only REQ0/GNT0 and REQ1/GNT1 pairs for external PCI devices. In the *X-board® Design Guide* you find additional information about how to expand these pairs by using certain devices on the backplane

Only INTA and INTB are externally available.

The ITE IT8152G companion chip maps all PCI interrupts to a single interrupt request line. This interrupt line is connected the GPIO[0] input of the Intel® XScale™ PXA255 interrupt controller.

10 Appendix C: Bootloader

10.1 Boot Loader

The boot loader is the low-level code that configures the X-board®<PXA> and loads the Windows CE .NET 4.2 image or any other operating system image. These images can be loaded from the Onboard Flash, Compact Flash or downloaded from Windows CE Platform Builder over an Ethernet connection. The boot loader code resides in Platform\xscxbd\eboot under the Windows CE .NET 4.2 root directory and the boot loader image (eboot.nb0) will be located in the same directory as your Windows CE Image nk.bin image. The boot loader image executes out of flash and the eboot.nb0 file is flashed into this ROM through a JTAG flash tool.

If it is necessary to modify the boot loader it is automatically built whenever a new Windows CE image is created. Please keep in mind that only a release version of the boot loader (created during a release Windows CE image build) should be flashed.

Note: *Never attempt to change the boot loader unless you have a working JTAG programmer and cable. If there's a problem with the boot loader code you will no longer be able to download new code and JTAG is the only means to revive the board.*

10.2 Boot Menu

During the boot process, the boot loader displays status information and a boot menu over the COM1 serial port. You can view this information and select menu items from a Windows host using the Microsoft HyperTerminal terminal emulation application. Use a null modem cable to connect the COM1 port of the X-board®<PXA> to your development workstation. This is the bottom connector on the Kontron X-board® Eval Backplane.

To configure HyperTerminal:

- From the Windows Start menu, choose All Programs and then choose Accessories.
- Choose Communications and then choose HyperTerminal.
- In the Connection Description dialog box, in the Name box, type a name for the connection to your X-board®<PXA>.
- From the Icon list, choose an icon to represent your connection and then choose OK.
- In the Connect To dialog box, in the Connect using box, choose the communications (COM) port on the development workstation through which you want to receive messages from the X-board®<PXA>.
- The COM port that you choose must be the COM port on the development workstation to which you attached the null modem cable.
- Choose OK.
- In the COM<Port Number> Properties dialog box, modify the settings for your connection so that the settings are correct for your BSP.

The following table shows the correct settings:

Bits per second	Data bits	Parity	Stop bits	Flow control
38400	8	None	1	None

```
Beginning System Initialization ...

         SDCLK[1]   = MemClk
         MemClk     = 99.53 MHz
         Run Mode   = 4 * MemClk
         Turbo Mode = Run Mode
         Mode:    RUN
         Flash = ?? MB, SDRAM = ?? MB

################################################################
##                Kontron XScale Bootloader                   ##
##                      XBD3R111.017                          ##
##              (C) Copyright 2004 Kontron                    ##
################################################################

Press [ENTER] to boot from flash
Press [SPACE] to open menu
Boot from flash after 5 seconds.
```

Pressing the Space key opens up the boot menu. Otherwise the board will process the auto menu select string or attempt to run the Windows CE Image from the onboard flash if no such string has been assigned.

```
### Boot Loader Configuration ###

<0> IP address:     192.168.35.224
<1> Subnet mask:    255.255.255.0
<2> DHCP:           Enabled
<5> Download image via CF Card
<7> Download image via RTL8139 PCI Ethernet
<t> Download image via RTL8139 BOOTP/TFTP
<u> Use Debug Ethernet: Disabled
<p> PCI Menu
<e> Erase Flash Menu
<d> Menu Delay:         5
<a> Menu Auto Select:   ""
<s> Save Configuration

Enter your selection:
```

Simply pressing the digit or letter will invoke the listed action.

<0> IP address

<1> Subnet mask

<2> DHCP

Option <2> allows you toggle between a fixed IP address and subnet mask and one provided by a DHCP server within your network. DHCP is enabled by default. If DHCP is disabled then options 0 and 1 allow you to assign fixed address.

```
Enter your selection: 0

Enter new IP address: 89.0.0.40
```

```
Enter your selection: 1

Enter new subnet mask: 255.255.255.0
```

<5> Download image via CF Card

Option <5> loads the image from a Compact Flash Card. See below for details.

<7> Download image via RTL8139 PCI Ethernet

Option <7> downloads the image from Platform Builder through the onboard Ethernet chip. See below for details.

<t> Download image via RTL8139 BOOTP/TFTP

Option <t> downloads the image from a BOOTP/TFTP server through the onboard Ethernet chip. This option offers the possibility to obtain a kernal image from a remote server. This is the most common way to setup a Linux environment.
Please contact Kontron Embedded Modules Technical Support for more information.

<u> Use Debug Ethernet

Option <u> toggles between enabling and disabling Debug Ethernet. If Debug Ethernet is disabled the onboard Ethernet chip can be used with the Standard Windows CE NDIS RTL8139 Ethernet driver. Ethernet Kernel Debugging, Messaging and CESH is then unavailable. If Debug Ethernet is enabled then the onboard Ethernet chip can be used with Platform Builder Ethernet Kernel Debugging, Messaging and CESH. The Windows CE image **MUST NOT** include the RTL8139 Ethernet driver. You can still access the network through the VMINI NDIS to Debug Ethernet Bridge Driver. This driver is included by default in the Windows CE Image.

<p> PCI Menu

Option <p> allows you to enter the PCI debug menu. In this menu you can find useful tools like ListPCIDevices or ReadPCICnfg (Read PCI Configuration Table) to debug the PCI devices on the backplane.

<e> Erase Flash Menu

Option <e> allows you to delete the content, or a part of it, from the onboard Flash. After you enter this menu you have the following possibilities:

<o> Erase OS image & registry from Flash

<r> Erase CE registry from Flash

<p> Erase CE registry & prevent registry saves until next OS image update.

<d> Menu Delay

Option <d> allows you to set the time period, in seconds, that the X-board®<PXA> will wait for the space key to be pressed to enter the boot configuration menu. The default is 5 seconds. If no key is pressed within that time the X-board®<PXA> processes the menu auto select string, or boots from flash, if no such string has been assigned.

<a> Menu Auto Select

Option <a> allows you to specify a menu auto select string. This is a series of key strokes that is automatically processed as menu selections when no real key is pressed during the menu delay period. For example, you might set this string to "u7" to automatically enable Ethernet Debugging and then immediately download the image through Ethernet. Set it to "5" to always boot from CF.

<s> Save Configuration

Option <s> saves the changes made to options 0, 1, 2, d, and a to EEPROM.

10.3 Booting from a Compact Flash

To load a Windows CE.net v4.2 image from Compact Flash you copy the nk.bin file to the Compact Flash card.

NOTE: *The Compact Flash card must be formatted for a FAT16 file system and the root partition must be made active. Select option 5 from the boot menu to load the image.*

10.4 Downloading an Image from Platform Builder

Before downloading a Windows CE image, make sure that you have the proper network setup such as DHCP, IP, and a subnet mask for the target platform.

➤ On the development workstation, from the Target menu, choose Configure Remote Connection.

- ➤ Choose the Services tab.
- ➤ From the Download box under Services for active named connection, choose Ethernet.
- ➤ Choose Configure.
- ➤ Power on the X-board®<PXA> and select option 7 from the boot menu.

After the X-board®<PXA> displays the "Sent BOOTME" messages, the device identification name of X-board®<PXA> (highlighted in the screen shot below) should automatically appear in the Available Devices list of the Platform Builder Configure Ethernet Download Dialog.

Note: *If the name of the X-board®<PXA> does not appear in the Available Devices list, reboot the X-board®<PXA>. If the name of the X-board®<PXA> still does not appear, verify that you made the correct changes.*

```
Enter your selection: 7

FlashVPPUp(); done
EraseRegFlash(); done
FlashVPPDown() done
goto DOWNLOAD
InitSpecifiedEthDevice(EthDevice = 6)
RTL8139 PCI card found: device 19, function 0
Ethernet Physical Base = 13E12000
Ethernet Virtual Base = BBE12000
RTL8139Init enter
RTL8139Init: ioaddr = 0xBBE12000
RTL8139CheckRam enter
RTL8139CheckRam exit
RTL8139Init:: MAC = 00-12-34-43-21-00
### Connection status: 10Mbps half-duplex ###
RTL8139InitDMABuffer enter
RTL8139InitDMABuffer exit
RTL8139Init exit
RTL8139 Ethernet controller initialized.
====== ISRTL8139PCICard == TRUE

Device identification: XSC1BD8448
InitDHCP():: Calling ProcessDHCP()
ProcessDHCP()::DHCP_INIT
Waiting for DHCP assignment...
ProcessDHCP()::DHCP IP Address Resolved as 89.0.0.40, netmask:
255.255.255.0
Lease time: 180000 seconds
Boot loop
Sent BOOTME to 255.255.255.255
Boot loop
Sent BOOTME to 255.255.255.255
Boot loop
Sent BOOTME to 255.255.255.255
Boot loop
Sent BOOTME to 255.255.255.255
```

- From the Available Devices list, select the name of the X-board®<PXA>, and then choose OK.
- From the Kernel Transport box, choose Ethernet.
- Choose the Settings tab.

You have now configured the services that allow you to connect to the target. You are now ready to establish a connection and download the OS image.

- From the Target menu, choose Download/Initialize.
- In the KITL Security Warning dialog box, choose Yes if you want the target device to have remote access to the file system on the development workstation.

If the X-board®<PXA> no longer sends the BOOTME messages you may have to reboot the board because the OS image does not download until it receives a BOOTME message and the X-board®<PXA> sends BOOTME messages for only a short period of time.

- Wait until the OS image downloads to the X-board®<PXA>.

While the OS image downloads, a dialog box in the IDE displays the progress of the download.

After the OS image successfully downloads and the OS boots, the desktop for the Windows CE OS appears on the display.

10.5 Downloading an Image from Platform Builder to Onboard Flash

Before downloading an image, make sure that you have the proper network setup such as IP, DHCP, and a subnet mask for the target platform.

You need to create a Windows CE Image specifically for Flash:

- In Platform Builder on the development workstation, from the Platform menu, choose Settings.
- Select the Build Options Tab.
- Check Enable Image for Flash
- Choose OK and Rebuild the Image.
- Then follow the same steps as in section 10.4, Downloading an Image from Platform Builder.

After the download the image will be flashed.

- Reboot the target after the flashing is complete.

11 Appendix d: X-board® connector pinouts

Pin number	Signal	Signal type	Pin number	Signal	Signal type
1	BUZZER	O_1	2	PWRGOOD_IN	I_2
3	N.C.		4	**V_BATT	I
5	Codec_SDATA_OUT	O_1	6	GPIO[14]	I/O
7	Codec_SDATA_IN	I_1	8	GND	P
9	Codec_BIT_CLK	I_I	10	GPIO[8]	I/O
11	Codec_SYNC	O_1	12	GPIO[12]	I/O
13	Codec_RESET#	O_1	14	GPIO[13]	I/O
15	GND	P	16	GND	P
17	Lan TX-	O_2	18	GPIO[10]	I/O
19	Lan TX+	O_2	20	GPIO[11]	I/O
21	Lan RX-	O_2	22	V33	P
23	Lan RX+	O_2	24	R5	O_1
25	Lan LNLED#	O_3	26	R4	O_1
27	Lan LNKLED#	O_3	28	R3	O_1
29	V33	P	30	R2	O_1
31	USB[1]+	O_{USB}	32	R1	O_1
33	USB[1]-	O_{USB}	34	R0	O_1
35	Overcurrent#	I_3	36	GND	P
37	USB[2]+	O_{USB}	38	G5	O_1
39	USB[2]-	O_{USB}	40	G4	O_1
41	GND	P	42	G3	O_1
43	DCD1#	I_1	44	G2	O_1
45	DSR1#	I_1	46	G1	O_1
47	RXD1	I_1	48	G0	O_1
49	RTS1#	O_1	50	V33	P
51	TXD1	O_4	52	B5	O_1
53	CTS1#	I_1	54	B4	O_1
55	DTR1#	O_1	56	B3	O_1
57	RI1#	I_1	58	B2	O_1
59	V33	P	60	B1	O_1
61	RXD2	I_1	62	B0	O_1
63	RTS2#	O_1	64	GND	P
65	TXD2	O_4	66	HSYNC	O_1
67	CTS2#	I_1	68	VSYNC	O_1
69	V33	P	70	DE	O_1
71	GPIO[1]	I/O	72	SCLK	O_{PC}
73	GND	P	74	GND	P
75	MMC_CMD	I/O	76	BIASON	I/O
77	MMC_DAT	I/O	78	DIGON	O_1
79	MMC_CLK	I/O	80	V33	P
81	GPIO[2]	I/O	82	V33-Standby	P
83	GND	P	84	Power Button#	I_1
85	AD[00]	I/O	86	Resume/Reset#	O_1
87	AD[01]	I/O	88	GPIO[4]	I/O
89	AD[02]	I/O	90	BATTLOW# (**)	I_1
91	AD[03]	I/O	92	GPIO Reset	I/O
93	AD[04]	I/O	94	PS_ON#	O_5
95	AD[05]	I/O	96	GPIO[9]	I/O
97	AD[06]	I/O	98	GND	P
99	AD[07]	I/O	100	LAD[3]	I/O
101	AD[08]	I/O	102	LAD[2]	I/O
103	C/BE[0]#	I/O	104	LAD[1]	I/O
105	AD[09]	I/O	106	LAD[0]	I/O

Pin number	Signal	Signal type	Pin number	Signal	Signal type
107	AD[10]	I/O	108	LDRQ#	I_4
109	AD[11]	I/O	110	LFRAME#	0_1
111	AD[12]	I/O	112	LPCPD#	0_1
113	AD[13]	I/O	114	SERIRQ#	$I/0_1$
115	AD[14]	I/O	116	V33	P
117	C/BE[1]#	I/O	118	USB[3]+ (USB Client)	0_{USB}
119	AD[15]	I/O	120	USB[3]- (USB Client)	0_{USB}
121	LOCK#	$I/0_1$	122	V33	P
123	PERR#	$I/0_1$	124	I2C_CLK	$I/0_2$
125	DEVSEL#	$I/0_1$	126	I2C_DAT	$I/0_2$
127	SERR#	$I/0_1$	128	GND	P
129	STOP#	$I/0_1$	130	IDE_DASP	$I/0_3$
131	CLKRUN#	-	132	IDE_PDIAG	$I/0_3$
133	TRDY#	$I/0_1$	134	V33	P
135	IRDY#	$I/0_1$	136	IDE_CS3#	$I/0_1$
137	FRAME#	I/O	138	IDE_CS1#	$I/0_1$
139	AD[16]	I/O	140	IDE_A2	$I/0_1$
141	C/BE[2]#	I/O	142	IDE_A0	$I/0_1$
143	AD[17]	I/O	144	IDE_A1	$I/0_1$
145	PAR	$I/0_1$	146	GND	P
147	AD[18]	I/O	148	IDE_INTRQ	I_8
149	AD[19]	I/O	150	IDE_AK#	$I/0_1$
151	AD[20]	I/O	152	IDE_RDY	$I/0_1$
153	AD[21]	I/O	154	IDE_IOR#	$I/0_1$
155	AD[22]	I/O	156	IDE_IOW#	$I/0_1$
157	AD[23]	I/O	158	IDE_DRQ	$I/0_1$
159	C/BE[3]#	I/O	160	GND	P
161	AD[24]	I/O	162	IDE_D0	$I/0_1$
163	AD[25]	I/O	164	IDE_D1	$I/0_1$
165	AD[26]	I/O	166	IDE_D2	$I/0_1$
167	AD[27]	I/O	168	IDE_D3	$I/0_1$
169	AD[28]	I/O	170	IDE_D4	$I/0_1$
171	AD[29]	I/O	172	V33	P
173	AD[30]	I/O	174	IDE_D5	$I/0_1$
175	GPIO[3]	I/O	176	IDE_D6	$I/0_1$
177	AD[31]	I/O	178	IDE_D7	$I/0_1$
179	REQ1#	I_6	180	IDE_D8	$I/0_1$
181	GNT1#	I_5	182	IDE_D9	$I/0_1$
183	REQ0#	I_6	184	IDE_D10	$I/0_1$
185	GNT0#	I_5	186	GND	P
187	RST#	0_1	188	IDE_D11	$I/0_1$
189	CLK1	0_1	190	IDE_D12	$I/0_1$
191	GPIO[5]	I/O	192	IDE_D13	$I/0_1$
193	GPIO[6]	I/O	194	IDE_D14	$I/0_1$
195	GPIO[7]	I/O	196	IDE_D15	$I/0_1$
197	INTA#	I_6	198	HDRST#	0_1
199	INTB#	I_6	200	GND	P

Note: ** If the LPC interface is not used on the customer's Backplane, the Signals LAD[0..3] and LDRQ# have to be connected together and pulled-up to 3.3V with an 15kΩ resistor*
*** don't use BATTLOW# to monitor RTC battery !*

➤ I1 Input, TTL compatible.

- I_2 Input, low active with open collector/button.
- I_3 Input, TTL compatible with Schmitt-Trigger. Internally pulled up (10kΩ) .
- I_4 Input, TTL compatible. Internally pulled up (10kΩ).
- I_5 Input, TTL compatible. Internally pulled down (4,7kΩ).
- I_6 Input, TTL compatible. Internally pulled up (2,7KΩ).
- O_1 Output 3,3V (3,14V-3,46V), source 2mA, sink 5mA.
- O_2 Output, differential pair.
- O_3 Output, open collector. 5V tolerant.
- O_4 Output. Do not pull up or down externally!
- O_{USB} Output. Internally pulled down (15kΩ).
- I/O Input/Output.
- I/O_1 Input/Output. Internally pulled up (2,7kΩ).
- I/O_2 Input/Output. Internally pulled up (10kΩ).
- P Power Input.

11.1 General purpose I/O's (GPIO's)

Pin no. (X-board®)	GPIO in X-board® Spec.	GPIO Signal used from PXA255	Alternative use *
71	GPIO[1]	GPIO[8] / MMCCS0	MMC Chip Select 0
81	GPIO[2]	GPIO[9] / MMCCS1	MMC Chip Select 1
175	GPIO[3]	GPIO[81] / NSSPCLK	Synchronous Serial Port Clock
88	GPIO[4]	GPIO[12] / 32kHz	32 kHz Clock / MMC card detect
191	GPIO[5]	GPIO[83] / NSSPTXD	Synchronous Serial Port Transmit Data
193	GPIO[6]	GPIO[84] / NSSPRXD	Synchronous Serial Port Receive Data
195	GPIO[7]	GPIO[82] / NSSPFRM	Synchronous Serial Port Frame
10	GPIO[8]**	Internal Use (**GPIO[5]** default) or (GPIO[49] / HWRXD)**	Internal Use (Hardware UART Receive Data)**
96	GPIO[9]	GPIO[2]	
18	GPIO[10]	GPIO[46] / IRRXD	IrDA Receive Data / Standard UART Receive Data
20	GPIO[11]	GPIO[47] / IRTXD	IrDA Transmit Data / Standard UART Transmit Data
12	GPIO[12]	GPIO[50] / HWCTS	Hardware UART Clear-To-Send
14	GPIO[13]	GPIO[51] / HWRTS	Hardware UART Request-To-Send
6	GPIO[14]	GPIO[48] / HWTXD	Hardware UART Transmit Data
1	BUZZER	GPIO[3]	
92	GPIO Reset	GPIO[1]	

Notes: ** Default configuration is GPIO functionality. Please check the Intel PXA255 Developers Manual for using the alternate function of these pins.*
*** GPIO[8] configurable by R404 and R405*

Configuration GPIO[8] on pin 10 (J1-Xboard connector)	R404	R405
GPIO[5] (from PXA)	not used	**used (default)**
GPIO[49] (from PXA) / HWRXD	used	not used

GPIO[49] (or alternative use HWRXD) is available when IDE interface of the X-board®<PXA> is not used, otherwise it is not available.

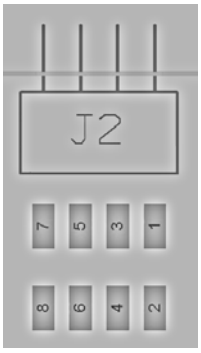
11.2 LCD Panel Pinout Table

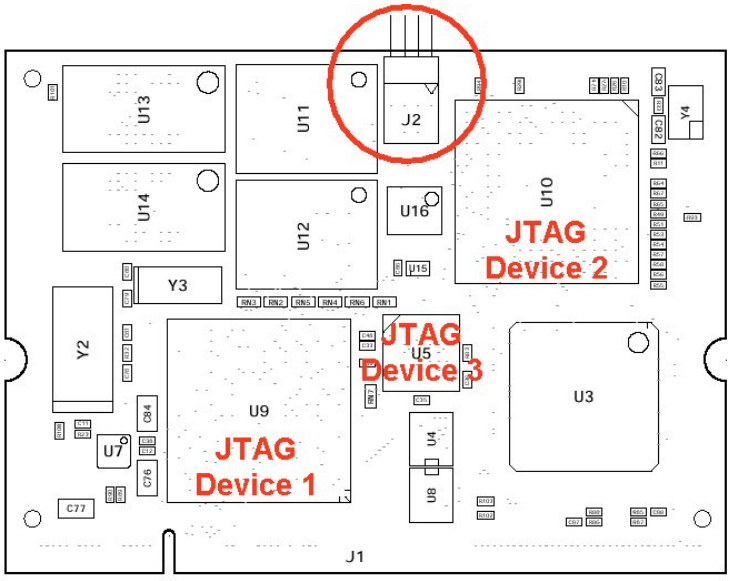
Pin no. (X-board®)	RGB Active Panel	Passive Single Panel Monochrome	Passive Single Panel Monochrome, Double Pixel	Passive Dual Panel Monochrome	Passive Color Single Panel	Passive Color Dual Panel
62	B0*					
60	B1	D3	D7	DU_3	D0	DU_0
58	B2	D2	D6	DU_2	D1	DU_1
56	B3	D1	D5	DU_1	D2	DU_2
54	B4	D0	D4	DU_0	D3	DU_3
52	B5		D3	DL_3	D4	DU_4
48	G0		D2	DL_2	D5	DU_5
46	G1		D1	DL_1	D6	DU_6
44	G2		D0	DL_0	D7	DU_7
42	G3					DL_0
40	G4					DL_1
38	G5					DL_2
34	R0					
32	R1					DL_3
30	R2					DL_4
28	R3					DL_5
26	R4					DL_6
24	R5					DL_7
72	SCLK	Pixel_Clock	Pixel_Clock	Pixel_Clock	Pixel_Clock	Pixel_Clock
66	HSYNC	Line_Clock	Line_Clock	Line_Clock	Line_Clock	Line_Clock
68	VSYNC	Frame_Clock	Frame_Clock	Frame_Clock	Frame_Clock	Frame_Clock
70	DE	BIAS	BIAS	BIAS	BIAS	BIAS

Note: **B0 and R0 are not supported by the PXA and therefore should to be connected to ground.*

11.3 JTAG Interface

The JTAG connector (J2) is not mounted by default on the X-board®<PXA>. For debug purposes a dual Pin row connector can be mounted on the module.





11.3.1 Specification and Pinout of the JTAG connector

4 x 2 pins; 1.27mm (0.050in) pitch; SMD

For Example: SAMTEC FTSH-104-02-L-DH

Pin No.	Signal	Description
1	#TRST	Test Interface Reset
2	VCC	Power Supply
3	TDO	Test Data Input
4	#SRST	System Reset
5	TMS	Test Mode Select
6	TDI	Test Data Output
7	TCK	Test Clock
8	GND	Ground

11.3.2 JTAG Chain

No	Device	IR Lenght
1	PXA255 (U9)	5
2	IT81526 (U10)	4
3	CPLD (U5) (Internal use!)	2

12 Appendix E: JIDA STANDARD

12.1 JIDA Information

To obtain information about boards that follow the JIDA standard refer to the JIDA32 Library API manual in the jidai114.zip folder, which is available from the Kontron Embedded Modules Web site, for further information on implementing and using JIDA calls with C sample code. The library itself is included in the BSP for the X-board®<PXA>.

Note: *The X-board®<PXA> only supports the JIDA32 Library API functions. The 16-bit legacy JIDA INT15 interface is tied to the x86 architecture and is* ***NOT*** *available on this board.*

13 Appendix F: PC Architecture Information

The following sources of information can help you better understand PC architecture.

13.1 Buses

13.1.1 Low Pin Count Bus (LPC)

- Low Pin Count Bus Specification, Aug. 2002, Intel

13.1.2 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

13.1.3 PCI/104

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

13.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8

- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

13.3 Ports

13.3.1 RS-232 Serial

- EIA-232-E standard:
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor:
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

13.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group:
  This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
  We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

13.3.3 USB

- USB Specification:
  USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

13.4 Programming

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

14 APPENDIX G: DOCUMENT-REVISION HISTORY

Filename	Date	Edited by	Alteration to preceding revision
XBD3M001.doc	04.12.03	C. Hoch	Initial Preliminary Release
XBD3M002.doc	17.12.03	D. Gunter	Added boat loader, watchdog configuration and LCD panel pinout table information.
XBD3M003.doc	12.02.04	D. Gunter	Added web site link to Technical Support section. Added notes about Watchdog and RTC limitations. Changed first listing of PIN 6 in General Purpose I/Os table to PIN 175.
XBD3M110.doc	11.05.04	C. Hoch	Added JTAG Interface, deleted RTC feature, changed environmental Spec., updated Bootloader
XBD3M111.doc	08.07.04	D. Gunter	Removed Battery information from section 6.
XBD3M112.doc	06.08.04	D. Gunter	Added information to section 10.2 about obtaining a kernal image for a remote server. Updated tables in sections 11.1 and 11.2
XBD3M113.doc	07.07.05	U. Geisler	Changed LCD Data-Pin Pixel Ordering for STN-Monochrome Panels X-board® connector PIN 3: AC97-clock is not connected
XBD3M114.DOC	24.10.05	U. Geisler	Added Ethernet limitation Corrected features of ITE8152G Released for WEB
XBD3M115.DOC		SAL	Corrected JTAG pin description (TDO/TDI) Added J2 detailed pin overview Reworked GPIO[8] description Removed RTC restriction, added V_BATT descr.
XBD3M116.DOC	01.12.2006	CMO	Added disclaimer and correct X-board® trademark
XBD3M117.DOC	03.07.2007	U. Geisler	Updated to current Kontron Layout